AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (previously presented) An array-type processor, comprising:

a multiplicity of processor elements which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, said multiplicity of processor elements being arranged in rows and columns;

a plurality of state control units that intercommunicate to realize linked operation as necessary; and

an event distributing means for distributing said event data to said plurality of state control units, said event distributing means comprising dedicated event communication lines that connect said plurality of state control units,

wherein said instruction codes of said multiplicity of processor elements are successively switched by said plurality of state control units in accordance with a computer program that has been installed in advance and in accordance with said event data, and

wherein said plurality of state control units comprises at least four state control units that are directly

interconnected to each other by respective dedicated event communication lines so that each of said at least four state control units is directly connected to all other ones of said state control units.

2-8. (canceled)

9. (previously presented) An array-type processor, comprising:

a multiplicity of processor elements which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, said multiplicity of processor elements being arranged in rows and columns;

a plurality of state control units that intercommunicate to realize linked operation as necessary;

an event distributing means for distributing said event data to said plurality of state control units; and

a central control unit for distributing said event data to said plurality of state control units, said central control unit is surrounded by said plurality of state control units and is connected by said event distributing means to all of said plurality of state control units,

wherein said instruction codes of said multiplicity of processor elements are successively switched by said plurality of state control units in accordance with a computer program that

has been installed in advance and in accordance with said event data.

10-14. (canceled)

15. (previously presented) An array-type processor, comprising:

a multiplicity of processor elements which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, said multiplicity of processor elements being arranged in rows and columns;

a plurality of state control units that intercommunicate to realize linked operation as necessary; and

an event distributing means for distributing said event data to said plurality of state control units,

wherein said instruction codes of said multiplicity of processor elements are successively switched by said plurality of state control units in accordance with a computer program that has been installed in advance and in accordance with said event data,

wherein said multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area and there is one state control unit for a plurality of processor elements,

wherein each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas, and

wherein said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units.

16-20. (canceled)

21. (new) An array-type processor in which a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes for which data is individually set and for which connection relations between the processor elements are switch-controlled, are arranged in rows and columns; and in which a state control means causes successive transitions of operating states in accordance with transition rules of a transition table memory; and in which said state control means successively switches said instruction codes of said multiplicity of processor elements in accordance with said operating states; wherein:

transitions of said operating states are done by a state control unit in accordance with a computer program that has been installed in advance and event data which are supplied by said multiplicity of processor elements;

said state control unit is composed of a plurality of units that intercommunicate to realize linked operation as necessary;

the multiplicity of said processor elements is divided into a number of element areas corresponding to the number of said plurality of state control units;

each of said plurality of state control units is connected to said processor elements corresponding to each of said plurality of state control units within respective element areas; and

said array-type processor includes an event distributing means for distributing said event data to said plurality of state control units that intercommunicate and realize linked operation.

22. (new) An array-type processor according to claim 21, wherein said event distributing means is constituted by dedicated event communication lines that connect said plurality of state control units.

23. (new) An array-type processor according to claim 21, wherein said event distributing means is constituted by dedicated event communication buses that connect said plurality of state control units.

24. (new) An array-type processor according to claim 21, wherein:

data buses for transmitting processing data of said plurality of processor elements are arranged in matrix form;

a plurality of switch elements, which switch-control a wiring configuration of said data buses in accordance with instruction codes that are individually set as data, are arranged in matrix form together with said processor elements;

said state control units successively switch said instruction codes of said plurality of processor elements and said plurality of switch elements; and

said event distributing means is constituted by said data buses that are switch-controlled by said switch elements.

25. (new) An array-type processor according to claim 22, wherein all of said plurality of state control units are interconnected by said event distributing means.

26. (new) An array-type processor according to claim 22, wherein:

said plurality of state control units are arranged in rows and columns; and

said state control units are connected by said event distributing means to a portion of said state control units that are located in a vicinity.

27. (new) An array-type processor according to claim 26, wherein said state control units are connected by said event distributing means to state control units that are located in eight directions in the vicinity.

28. (new) An array-type processor according to claim 26, wherein said state control units are connected by said event distributing means to said state control units that are adjacent in four row and column directions.

29. (new) An array-type processor according to claim 26, wherein a central control unit is provided for distributing said event data to said plurality of state control units; and said central control unit is connected by said event distributing means to all of said plurality of state control units.

30. (new) An array-type processor according to claim 21, wherein an input selection means is provided for each of said state control units for selecting one from said plurality of items of event data that are simultaneously received as input by said event distributing means.

31. (new) An array-type processor according to claim 26, wherein an input selection means is provided for each of said state control units for selecting one from said plurality of items of event data that are simultaneously received as input by said event distributing means.

32. (new) An array-type processor according to claim 21, wherein one item of said event data that has been selected by said input selection means is supplied as output to said event distributing means.

33. (new) An array-type processor according to claim 21, wherein output selection means is provided for each of said

state control units, said output selection means selecting one from a plurality of items of said event data that are simultaneously received as input by said event distributing means and supplying these event data as output to said event distributing means.

34. (new) An array-type processor according to claim 26, wherein:

said multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area;

each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas; and

said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units.

35. (new) An array-type processor according to claim 21, wherein:

said multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area;

each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas; and

said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units.